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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/325,882	06/04/1999	DAVID E. SINCLAIR	0100.9900390	3412

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EXAMINER	
KIM, HAROLD J	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 05/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/325,882	SINCLAIR ET AL.	
	Examiner	Art Unit	
	Harold Kim	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This Office Action is in response to the filing of the Amendment A, Paper # 4, on 3/12/02, has been considered but the arguments are moot in view of the new ground(s) of rejection. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, this action is made **FINAL**.

2. Claims 1-16 are presented for examination.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-3, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones, Jr., US Patent no. 5,781,768, in view of Houston, US Patent no. 6,307,281.

6. In re claim 1, Jones, Jr. shows a power consumption reduction circuit [fig 4] comprising:

a memory clock source [5, figs 1] for a graphic controller [fig 1; abstract]; and

a memory clock divider circuit [fig 4], operative to the memory clock source, that generates divided memory clock output signals as a plurality of corresponding independent clock signals to a memory interface circuit [col 12, claim 2]. Jones, Jr. also shows the plurality of corresponding independent clock signals to a number of interfaces for processing engines and activates the plurality of independent clock signals in response to received condition data during an active mode [fig 4].

Jones, Jr. does not show the plurality of corresponding independent clock signals to a number of interface circuits for differing processing engines and selectively activates at least some of the plurality of independent clock signals in response to received condition data during an active mode. Houston, 6,307,281, shows the plurality of corresponding independent clock signals [Houston, 6,307,281, col 12, claim 2] to a number of interface circuits for differing processing engines and selectively activates at least some of the plurality of independent clock signals in response to received condition data during an active mode [Houston, 6,307,281, col 12, claim 2; col 3, lines 1-7]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the plurality of corresponding independent clock signals to a number of interface circuits for differing processing engines and selectively activates at least some of the plurality of independent clock signals in response to received condition data during an active mode as shown in Houston for reducing power without impacting the operation of the rest of the circuit [Houston, 6,307,281col 3, lines 5-7].

7. In re claim 2, Jones, Jr. shows an engine clock source [5, fig 1] operatively coupled to a switching circuit [4, fig 1] that generates an output clock signal [output from 4 in fig 1] that is selectively coupled as a clock signal [fig 4] based on standby mode data [col 4, lines 5-9].

Jones, Jr. does not show a video overlay engine, a video capture engine, I2C control logic and a multimedia. Official Notice is taken that the video overlay engine, the video capture engine, I2C control logic and a multimedia port are old and well known in the art. Therefore, it would have been obvious to the ordinary skilled person in the art at the time the invention was made to modify the device to include the video overlay engine, the video capture engine, I2C control logic and a multimedia port for purpose of user friendly and more flexible device by allowing it to operate in multiple configurations.

8. In re claim 3, Jones, Jr. shows a variable memory clock control circuit [4, fig 4] based on type of memory request [col 3,lines 8-66].

9. In re claim 7, Jones, Jr. shows the claimed invention in fig 4.

10. Claims 4-6, and 8-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones, Jr., US Patent no. 5,781,768, in view of Houston, 6,307,281, and in further view of Houston, US Patent no. 5,544,101.

11. In re claims 4-6, the combination of Jones, Jr. and Houston, 6,307,281 does not show a plurality of memory read latch circuits and a memory read latch control circuit operative to dynamically activate and deactivate the plurality of memory read latches based on detected memory read requests to facilitate memory access activity based power reduction, the memory read latch control circuit generates a read latch enable

signal, a read data latency compensation circuit, a gating circuit responsive to the read latch control signal and a memory clock signal operative to selectively enable and disable memory read latches as a function of memory requests, a multiplexer having a output operatively coupled to the gating circuit, a first input coupled to receive the memory clock signal, and a second input coupled to receive a memory clock feedback signal wherein the multiplexer is controlled to output the memory clock signal.

Houston, 5,544,101, shows a plurality of memory read latch circuits and a memory read latch control circuit operative to dynamically activate and deactivate the plurality of memory read latches based on detected memory read requests to facilitate memory access activity based power reduction, the memory read latch control circuit generates a read latch enable signal, a read data latency compensation circuit, a gating circuit responsive to the read latch control signal and a memory clock signal operative to selectively enable and disable memory read latches as a function of memory requests, a multiplexer having a output operatively coupled to the gating circuit, a first input coupled to receive the memory clock signal, and a second input coupled to receive a memory clock feedback signal wherein the multiplexer is controlled to output the memory clock signal [fig 1]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a plurality of memory read latch circuits and a memory read latch control circuit operative to dynamically activate and deactivate the plurality of memory read latches based on detected memory read requests to facilitate memory access activity based power reduction, the memory read latch control circuit generates a read latch enable signal, a read data latency

compensation circuit, a gating circuit responsive to the read latch control signal and a memory clock signal operative to selectively enable and disable memory read latches as a function of memory requests, a multiplexer having a output operatively coupled to the gating circuit, a first input coupled to receive the memory clock signal, and a second input coupled to receive a memory clock feedback signal wherein the multiplexer is controlled to output the memory clock signal as shown in Houston, 5,544,101 to the combination for the purpose of power saving.

12. Claims 8-16 are rejected under the same rationale as discussed above in claims 1-7.

Conclusion

Applicant's arguments with respect to claims 1-16 have been considered but they are moot in view of the new ground(s) of rejection. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 746-7239 for regular communications (for informal or draft communications, please label "PROPOSED" or "DRAFT"), and

(703) 746-7238 for After Final communications.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to the technology center receptionist whose telephone number is (703) 306-5631.

Direct any inquiries concerning drawing review to the Drawing Review Branch (703) 305-8404.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harold Kim whose telephone number is (703) 305-1948. The examiner can normally be reached on Monday-Thursday 6 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on (703) 308-3301.

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Harold J. Kim
Patent Examiner
May 22, 2002/HK